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Development of quantum device simulator NEMO-VN1

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Abstract. We have developed NEMO-VN1 (NanoElectronic MOdelling), a new modelling tool that simulates a wide variety of quantum devices including Quantum Dot (QD), Resonant Tunneling Diode (RTD), Resonant Tunneling Transistor (RTT), Single Electron Transistor (SET), Molecular FET (MFET), Carbon Nanotube FET (CNTFET), Spin FET (SPINFET). It has a collection of models that allow user to trade off between calculation speed and accuracy. NEMO-VN1 also includes a graphic user interface of Matlab that enables parameter entry, calculation control, intuitive display of calculation results, and in-situ data analysis methods.

Keywords: Quantum device, single electron transistor, nanoelectronic modelling.

1. Introduction

The dimensional scaling of CMOS device and process technology will become much more difficult as the industry approaches 10 nm around the year 2020 and will eventually reach asymptotic end according to the International Technology Roadmap for Semiconductor for emerging research devices [1]. Beyond this period of traditional CMOS it may be possible to continue functional scaling by integrating an alternative electronic device on to a silicon platform. These alternative electronic devices in the future include 1D structures (such as CNTs and compound semiconductor nanowires), RTDs, SET, molecular and spin devices, all of which are discussed in this work.

Despite these exciting possibilities, nanoelectronic devices are still in their relative infancy. The expense and difficulty of device fabrication precludes simply building and testing vast arrays of quantum devices. To focus efficiently on the best design, engineers need a tool that predicts electronic characteristics as a function of the device geometry and composition. In the more scientific mode, such a simulator would greatly enhance the understanding of quantum effects that drive the transport process and provide a means to investigate new device concepts.

Even conventional devices require a correction for quantum effects associated with the smaller device features. MOS devices, for example, exhibit electron confinement effects in the inversion layer. This phenomenon is a function of decreasing oxide thickness rather than the overall size of the device. Quantum effects become important as the oxide layer thickness decreases below 2 nm, which will soon be a standard for manufactured integrated circuits. Problems of this nature will become more prevalent as device geometries continue to shrink.

Nanoelectronic device modelling requires a fundamental quantum-mechanical approach. Many forms of quantum correction to classical electronic device models have been proposed or implemented. These include MOSFET-specific quantum corrections [2, 3] and generic quantum corrections to the drift-diffusion [4], hydrodynamic [5], and Boltzmann transport equation models [6]. Therefore, the semiconductor industry needs a new fully quantum-mechanically based TCAD (technology computer aided design) tool.

To address this problem, we developed a general purpose quantum device simulator called NEMO-VN1 (NEMO in Vietnam). NEMO-VN1 can simulate a wide variety of nanoelectronic devices, including QD, RTD, RTT, SET, MFET, CNFET and SPINFET. It has a collection of models that allow user to trade off between calculation speed and accuracy. NEMO-VN1 also includes a graphic user interface (GUI) of Matlab that enables parameter entry, calculation control, display of calculation results, and in-situ data analysis methods.

This work reviews the capabilities of NEMO-VN1, summarize the theoretical approach and experimental results, and give examples of typical NEMO-VN1 simulations.

2. Simulation results

2.1. NEMO-VN1 GUI

2.1.1. Overview

Another important goal of the NEMO-VN1 project was to make a user-friendly simulator that provides as much control as possible over every aspect of the simulation. Flexibility and ease of use are difficult to achieve simultaneously, but given the complexity of quantum device simulations it became clear that both criteria were vital to program success. Consequently, GUI development was major part of the NEMO-VN1 program. Here we present an overview of the most important GUI features, including:

- Main Screen
- Resonant Tunnelling Diode (RTD)
- Resonant Tunnelling Transistor (RTT)
- Quantum Dot (QD)
- Quantum Well (QWe)
- Quantum Wire (QWi)
- Single Electron Transistor (SET)
- Carbon Nanotube Field Effect Transistor (CNTFET)
- Molecular Field Effect Transistor (MFET)
- Spin Field Effect Transistor (SPINFET)

2.1.2. Main screen

NEMO-VN1 has a rich variety of simulation models, while this provides the maximum flexibility in terms of applicability to different types of devices and test conditions. The problem is that NEMO-VN1 requires over 100 simulation parameters. Traditional device simulators force the users to familiarize themselves with all available simulation parameters and ensure that they are set correctly. To minimize this burden for the users, NEMO-VN1 uses a hierarchical approach to input and displays simulation parameter values. The top level of this hierarchy specifies the highest level option (type of device). Subsequent levels contain more detailed options such as current-voltage characteristics of devices, types of material, size of devices, size of barriers, temperature, colours, etc.

The main screen shown in figure 1a is the central location where the user controls the NEMO-VN1 simulation. From main screen, the user can choose various types of quantum device simulations by clicking the mouse pointer on component items (left top corner). In this manner, the user can quickly enter the device list with minimum of typing. Double clicking the left mouse pointer on each item in

the device list initiates the selection of models which is used to calculate the current voltage characteristics (figure 1b).

(a) (b)

Figure 1. a) The NEMO-VN1 main screen. File of components contains a device list. b) Pressing left mouse pointer on "components" displays a list of simulation quantum devices.

2.2. NEMO-VN1 simulations

In the course of the NEMO-VN1 program, we have simulated QD, QWi, QWe, RTD, RTT, SET, CNTFET, MFET, and SPINFET. As examples, in the following sections, we consider current voltage characteristics of these quantum devices.

2.2.1. RTD and RTT simulations

Resonant tunnelling devices - Resonant tunnelling devices for logic applications include RTTs and hybrid devices incorporated with RTDs and one or more FETs (RTD-FET). The RTDs are two terminal devices that have a very high switching speed and exhibit a region of negative differential resistance in their I-V curves. These two characteristics make them potentially attractive as high-speed switching devices.

Adding a control terminal to RTDs extends their usability to a variety of applications. This approach has been used to build RTT. RTTs have a negative transconductance that can be used in several logic circuits, e.g., in XOR gate with only one transistor.

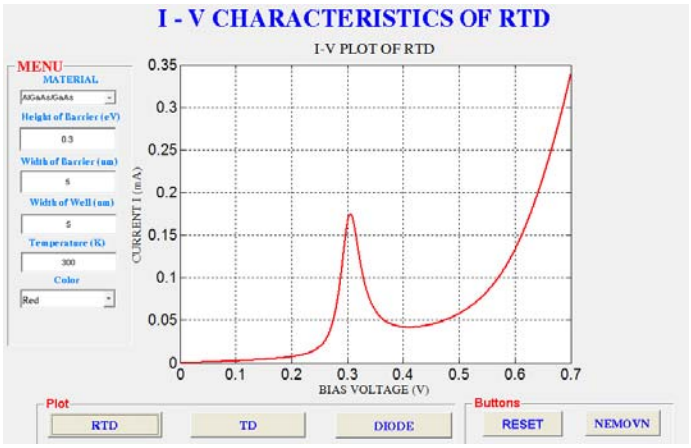
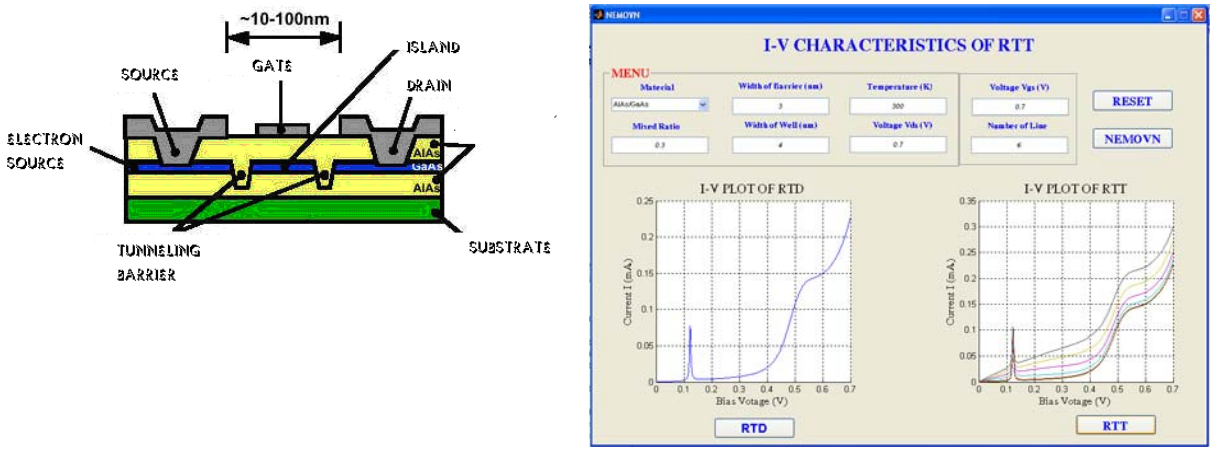


Figure 2. NEMO-VN1 plots current voltage characteristics for 2-barrier RTD device. The DC bias is applied and current is measured as a function of bias voltage at 300 K. For this device, RTD is formed on AlGaAs/GaAs, height of barrier is 0.3 eV, width of barrier is 5 nm, width of well is 5 nm.

Traditionally, RTDs have been fabricated in III-V material systems that has limited widespread their applicability. Recently, several papers have described fabrication of group IV devices with silicon compatible materials. Overall, the resonant tunnelling devices may be used for certain applications requiring high speed and low dynamic range and low peak currents provided the manufacturing issues associated with uniformity of the tunnelling barrier can be resolved. The principle focus of the recent research activity involving RTDs has been in the area of integration on the silicon platform. The current voltage characteristics of RTD are shown in figure 2.

In fact, there are two approaches for RTT model (hybrid RTD-FET) that can be described as follows. RTD is connected with FET in series or in parallel. Here we use the later configuration. The model of RTT is displayed in figure 3a. Current voltage characteristics are shown in figure 3b.



(a) (b)

Figure 3. a) The model of RTT, b) NEMO-VN1 plots current voltage characteristics for RTT device. The drain current is measured as a function of gate voltage (right). The current voltage characteristic of RTD is used for comparison (left).

The algorithm for the calculation of drain current of RTD in the model can be described as follows. Because of the small size of these devices, and the near one-dimensional nature of charge transport within them, RTD modelling demands a rigorous quantum-mechanical basis. This is achieved in this model by using the effective-mass Schrödinger equation to compute transport function of electrons, and by using transport function to compute the source-drain current. Total current can be obtained by summing current of RTD and current of nFET.

2.2.2. SET simulations

Single electron transistors - SETs are three-terminal switching devices that can transform electrons from source to drain one by one. Potentially, they can deliver high device density and power efficiency at good speed if the issues of noise immunity and low fan-out can be solved.

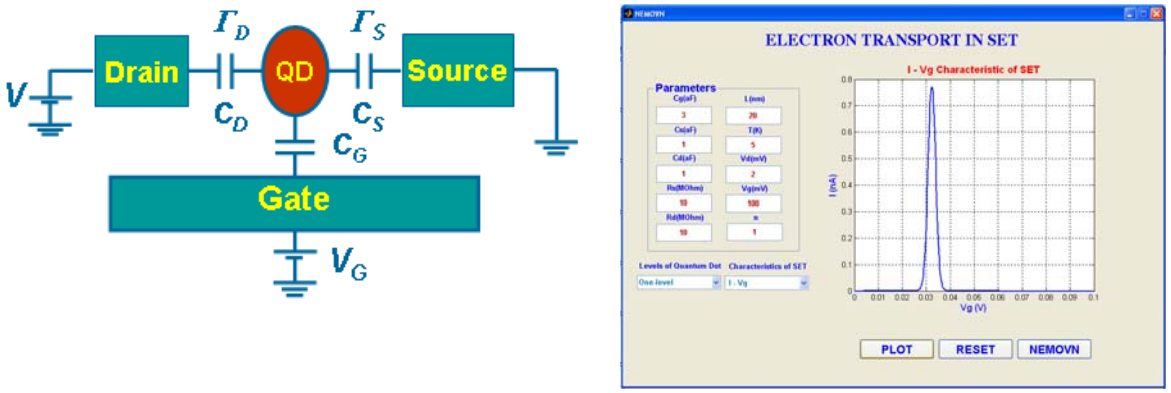
The structure of SETs is almost the same as that of FETs. The important difference, however, is that in a SET the channel is separated from source and drain by tunnelling junctions, and the role of the channel is played by a QD. Operational parameters of SETs depend on the size of QD. Single electron devices operating at room temperature were experimentally demonstrated. However, operation of complex and fast SET logic circuits is generally limited to very low temperatures due to low noise immunity.

The algorithm for the calculation of drain current in the model can be described as follows. Because of the small size of these devices, and the near one-dimensional nature of charge transport within them, SET modelling demands a rigorous quantum-mechanical basis. This is achieved in this model by using QD model to compute electro-chemical potential, density of electron states, Fermi-Dirac distribution and to compute the drain current. The model of SET is displayed in figure 4a. Current voltage characteristics are shown in figure 4b.

2.2.3. CNTFET simulations

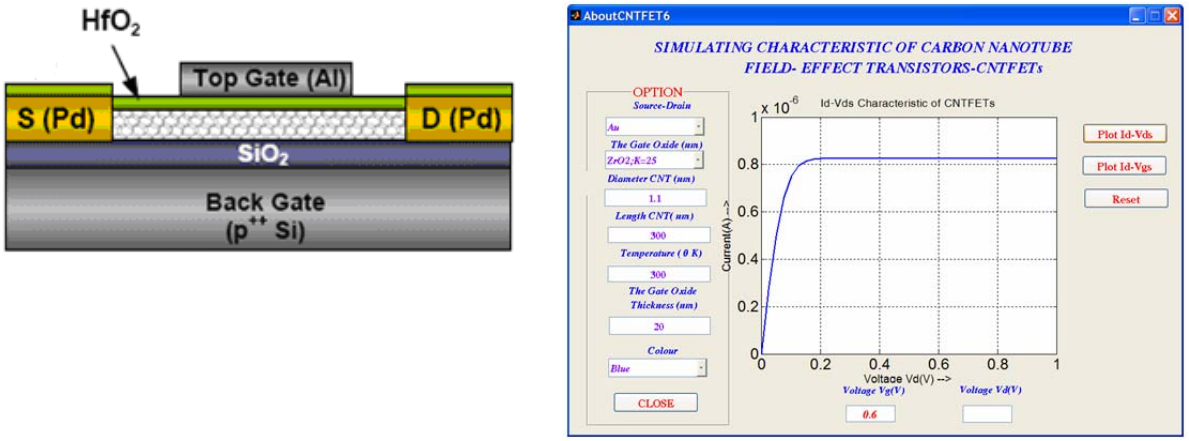
1D structures (Carbon Nanotubes and Nanowires) - Recently, the research activity in this area has matured to the point where one can identify the critical problems associated with 1D structures. The activities have centred around four main poles: 1) understand the basic physical mechanisms at work in quantum confined transport including coherent transport; 2) synthesize nanotubes and nanowire

materials with predictable and controllable characteristics; 3) address device fabrication issues like placement, contacting, doping, dielectric and gate material integration issues; and lastly, 4) characterize device issues such as transport efficiency, subthreshold slope, ambipolar conduction, RF response, I_{ON}/I_{OFF} ratios and others.



(a) (b)

Figure 4. a) Circuit model of SET. The QD is connected to the source and drain electrodes through small tunnel barriers. The potential in the QD can be modified by gate electrode which is capacitive coupled to the QD. The DC bias (V) is applied and the current is measured as a function of the V and V_g. b) Coulomb blockage oscillations of SET. The current is measured at 5 K as a function of the gate voltage. For this device, $C_G = 3$ aF, $C_S = 1$ aF, $C_D = 1$ aF, V = 2 mV.



(a) (b)

Figure 5. a) The model of CNTFET, b) NEMO-VN1 plots current voltage characteristics for CNTFET. Current is measured as a function of drain voltage at 300 K. For this device, source-drain of CNTFET is made of Au, diameter of CNT is 1.1 nm, length of CNT is 300 nm, gate thickness is 20 nm.

Significant progress has been made in the synthesis of nanotubes with controllable properties through the use of plasma enhanced chemical vapour deposition. It is now possible to produce nanotubes, over 90% of which have semiconductor properties. While this is a long way from the purity requirements in manufacturing settings, it does represent significant progress.

One of the fabrication challenges associated with CNT-FETs is reliable positioning and growth of nanotubes at lithographically defined sites.

The algorithm for the calculation of drain current in the model can be described as follows. Because of the small size of these devices, and the near one-dimensional nature of charge transport within them, CNFET modelling demands a rigorous quantum-mechanical basis. This is achieved in

this model by using non-equilibrium Green's function method to compute transport of the electron and hole charges in nanotubes, and by using the Landauer equation to compute the drain current. The model of CNT-FET is displayed in figure 5a. Current voltage characteristics are shown in figure 5b.

The current voltage curve can be divided into two regions: linear and saturation. Drain current in the linear region of CNTFET can be described as follows:

$$I_d = \frac{W}{L}\mu C_{ox}[(V_{gs} - V_T)V_{ds} - \frac{V_{ds}^2}{2}] \quad (1)$$

or

$$I_d = K_n\left[2(V_{gs} - V_T)V_{ds} - V_{ds}^2\right], \quad (2)$$

where K_n is conductance of CNTFET, W is the width of CNTFET, L is the length of CNTFET, μ is the mobility of carriers, C_{ox} is oxide gate capacitance.

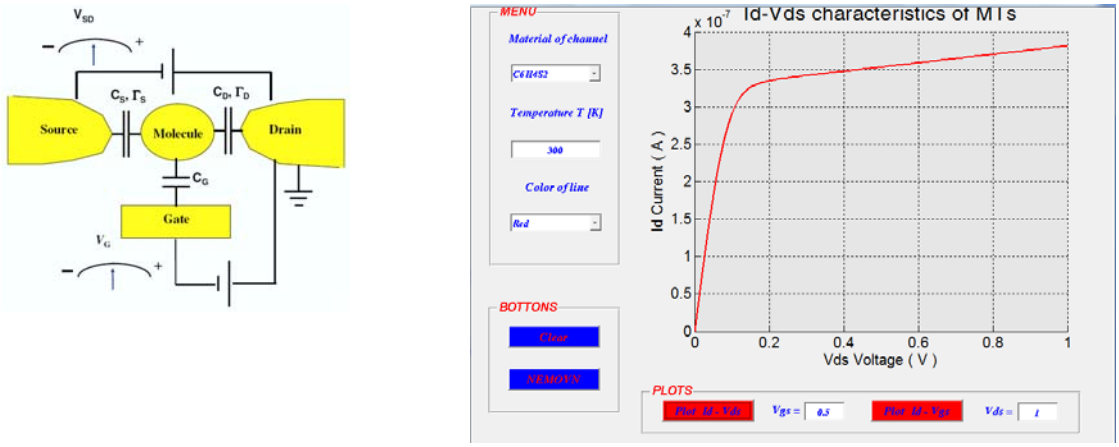
We can also obtain saturation current of CNTFET by replacing $V_{ds(sat)} = V_{gs} - V_T$. Then the expression of saturation current of CNTFET can be written:

$$I_{d(sat)} = K_n(V_{gs} - V_T)^2 \ . \quad (3)$$

2.2.4. MFET simulations

Molecular devices –The concept of molecular electronic devices is based on electronic properties of individual molecules tailored to perform logic operations and on the assembly of a large number of these functional building blocks into molecular circuits. Logic functions can be provided by electron transport and controlled switching behaviour of the molecules and may involve designated energy levels and charge states. Two-terminal devices such as resistive switches as well as three-terminal devices such as gated, transistor-like molecules are envisioned. The integration of these molecules into circuits requires the fabrication of contacts with atomic level precision and involves organic or inorganic interconnects on nanometer scale.

Many attempts have been made to build and characterize single molecular electronic devices, mainly since the mid-1990. Molecular functions that have been reported include rectifications, controlled conduction through gating as well as switching. Typically, these results have been obtained in mechanical break junction experiments or by scanning probe techniques.



(a) (b)

Figure 6. a) Circuit model of MFET. b) NEMO-VN1 plots current voltage characteristics for MFET. For this device, material is benzene. The drain current is measured as a function of V_{ds} at fixed voltage, V_g.

The algorithm for the calculation of drain current in the model can be described as follows. Because of the small size of these devices, and the near one-dimensional nature of charge transport

within them, MFET modelling demands a rigorous quantum-mechanical basis. This is achieved in this model by using non-equilibrium Green's function method to compute transport of the electron and hole charges in the molecular, and by using the transport function to compute the drain current. The model of MFET is displayed in figure 6a. Current voltage characteristics are shown in figure 6b.

The current voltage curve of MFET can be divided into two regions: linear and saturation. Drain current of MFET can be described as follows:

$$I_d = \frac{W}{L}\mu C_{ox}[(V_{gs} - V_T)V_{ds} - \frac{V_{ds}^2}{2}] \tag{4}$$

or

$$I_d = K_n\left[2(V_{gs} - V_T)V_{ds} - V_{ds}^2\right], \tag{5}$$

where K_n is conductance of MFET, W is the width of CNTFET, L is the length of CNTFET, μ is mobility of carriers, C_{ox} is oxide gate capacitance.

We can also obtain saturation current of MFET by replacing $V_{ds(sat)} = V_{gs} - V_T$. Then the expression of saturation current of MFET can be written:

$$I_{d(sat)} = K_n(V_{gs} - V_T)^2 + \alpha V_{ds}\ , \tag{6}$$

where α is the slope of drain current in saturation region. Here coefficient α equals 75 nA/V.

2.2.5. SPINFET simulations

Spin devices **-** They include a novel MOSFET. This device consists of a MOS gate structure and half-metallic ferromagnetic contacts for the source and drain. Other devices include spin torque transistor, magneto-resistive element (MRE), and spin gain transistor. The spin MOSFET uses a high spin polarized source in conjunction with spin dependent scattering in the drain as spin dependent effects that augment the gate controlled electrostatic transport in heterojunction MOSFET. The resulting hybrid device combines the electrostatic and spin dependent control of the drain current to provide a device concept, which in theory meets several important criteria. Spin MOSFET devices have been simulated to show the above criteria but no experimental demonstration has been published. The principal experimental difficulties will likely centre on the half-metal source-drain materials and problem with injection of spin-polarized electrons into the channel.

The "spin torque transistor" is based on the experimentally verified spin torque effect to modulate a source-drain current flow. This device concept has been reduced to practice and it is quite illustrative of the extended device functionalities created by the fundamental interplay between electric charge and electronic spin. It also illustrates that new materials can play the role in alternative logic technologies beyond CMOS. The "spin gain transistor" is based on experimentally observed and theoretically understood carrier mediated ferromagnetic phase transitions in dilute magnetic semiconductors. This device is similar to a magnetic bipolar transistor, where spin gain is achieved via creation of condition for the ferromagnetic transition. Spin gain in this case is defined to be the ratio of spin polarized (for example, spin up) electrons in collector current relative to the number of spin up electrons in the base. This concept has not been experimentally demonstrated. The MRE devices utilize four or more magneto-resistive junctions, each one of which is composed of a hard magnetic layer used for reference and a soft magnetic layer that can switch polarity dependent on the magnitude and direction of current in two input line. If the magnetic layers are aligned, the resistance of the junction is low and if the magnetic layers are anti-parallel, the resistance will be high.

A few concepts have emerged as indicted above but so far, no viable devices have been demonstrated, but the field of spin transistors is the subject of a great deal of continuing research activity. The algorithm for the calculation of drain current in the model can be described as follows. Because of the small size of these devices, and the near one-dimensional nature of charge transport within them, SPINFET modelling demands a rigorous quantum-mechanical basis. This is achieved in this model by using non-equilibrium Green's function method to compute transport function of

electrons, and by using transport function to compute the drain current. The model of SPINFET is displayed in figure 7a. Current voltage characteristics are shown in figure 7b.

The current voltage curve can be divided into two regions: linear and saturation. Drain current in the linear region of SPINFET can be described as follows:

$$I_d = \frac{W}{L}\mu C_{ox}[(V_{gs} - V_T)V_{ds} - \frac{V_{ds}^2}{2}] \quad (7)$$

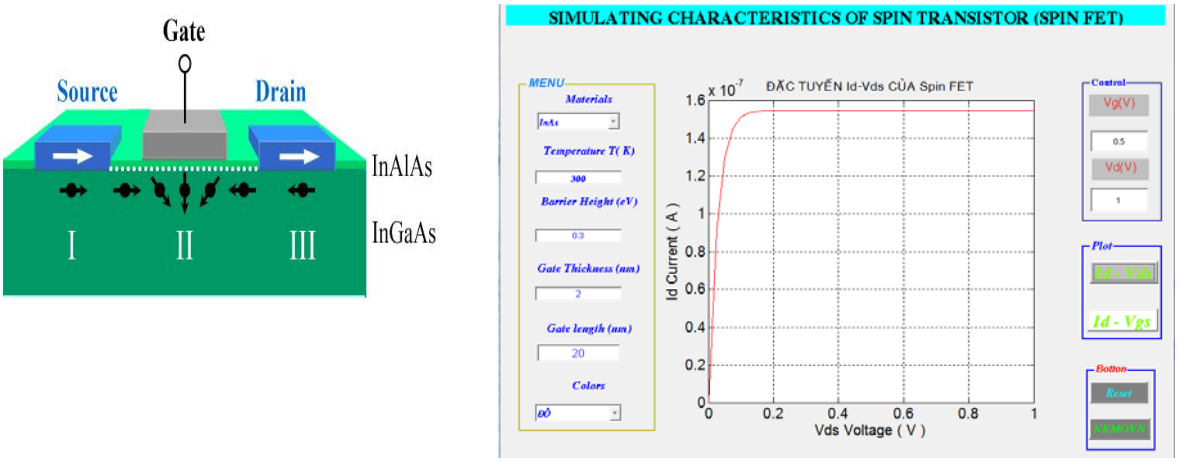
or

$$I_d = K_n\left[2(V_{gs} - V_T)V_{ds} - V_{ds}^2\right], \quad (8)$$

where K_n is conductance of SPINFET, W is the width of CNTFET, L is the length of CNTFET, μ is the mobility of carriers, C_{ox} is oxide gate capacitance.

We can also obtain saturation current of SPINFET by replacing $V_{ds(sat)} = V_{gs} - V_T$. Then the expression of saturation current of SPINFET can be written:

$$I_d = K_n\left[(V_{gs} - V_T)^2\right]. \quad (9)$$



(a) (b)

Figure 7. a) Model of SPINFET. b) NEMO-VN1 plots current voltage characteristics for SPINFET. The drain current of SPINFET is measured at 300 K as a function of V_g and V_{ds}. For this device, material is InAs, height of barrier is 0.3 eV.

3. Conclusions

We have created a comprehensive, versatile and user-friendly quantum device modelling tool. The simulator has predictive capability that we have tested for a number of materials and different devices.

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